



TYN20B-600T

SCR

21 March 2014

Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT404 (D2PAK) surface mountable plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)} = 150\text{ °C}$).

2. Features and benefits

- High bidirectional blocking voltage capability
- High junction operating temperature capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Very high current surge capability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

Table 1. Quick reference data

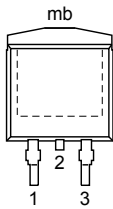

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	210	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	231	A
T_j	junction temperature		-	-	150	°C



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 129\text{ °C}$; Fig. 2 ; Fig. 3	-	-	20	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7	-	4.5	32	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 150\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	300	-	-	V/ μ s

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>D2PAK (SOT404)</p>	 <p>sym037</p>
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TYN20B-600T	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
TYN20B-600T	TYN20B-600T

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 129\text{ }^{\circ}\text{C}$; Fig. 1	-	12.7	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 129\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3	-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	210	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	231	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	220.5	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 40\text{ A}$; $I_G = 200\text{ mA}$; $di_G/dt = 200\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	5	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	150	$^{\circ}\text{C}$

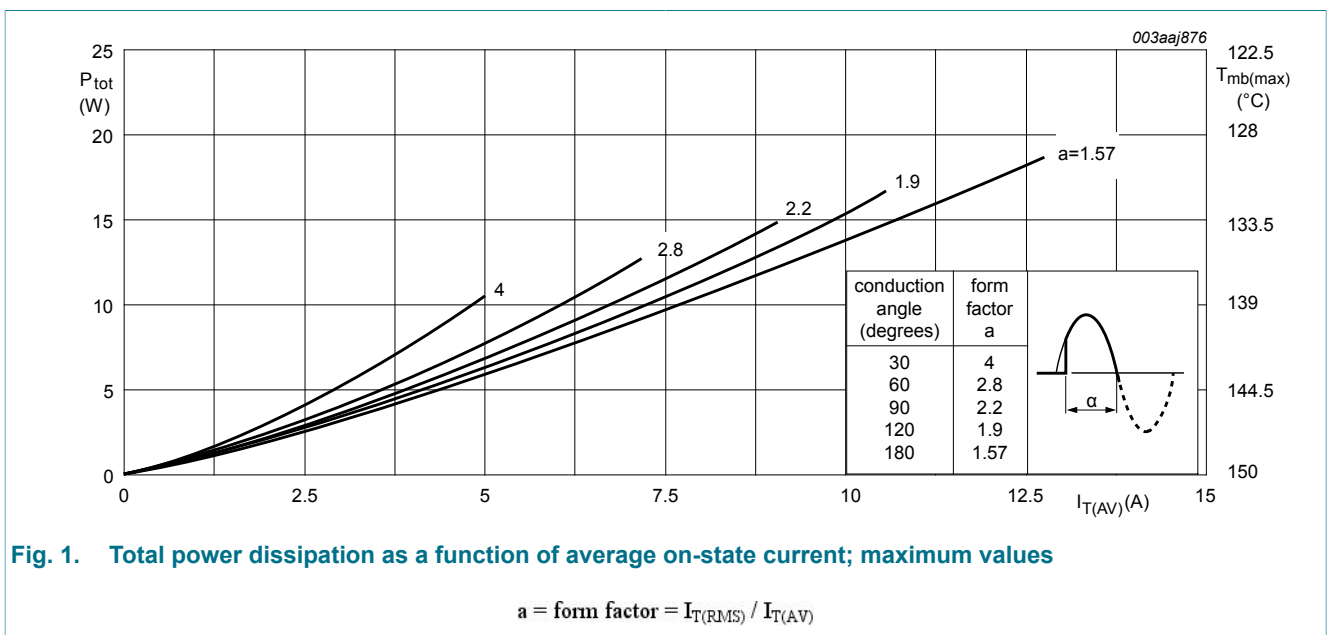


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

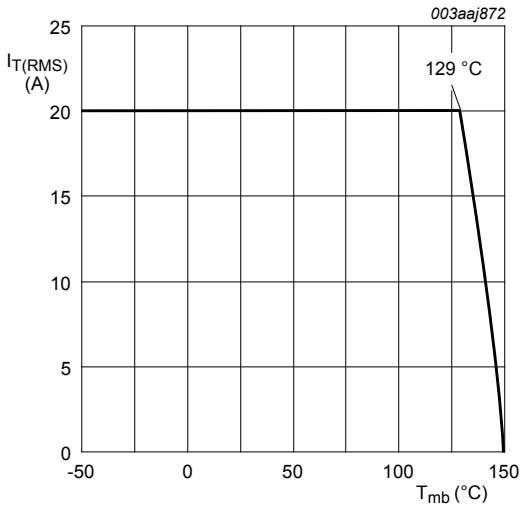


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

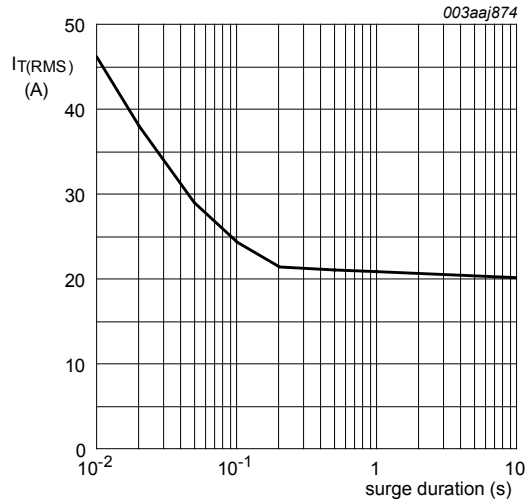


Fig. 3. RMS on-state current as a function of surge duration; maximum values

$f = 50 \text{ Hz}; T_{mb} = 129 \text{ }^\circ\text{C}$

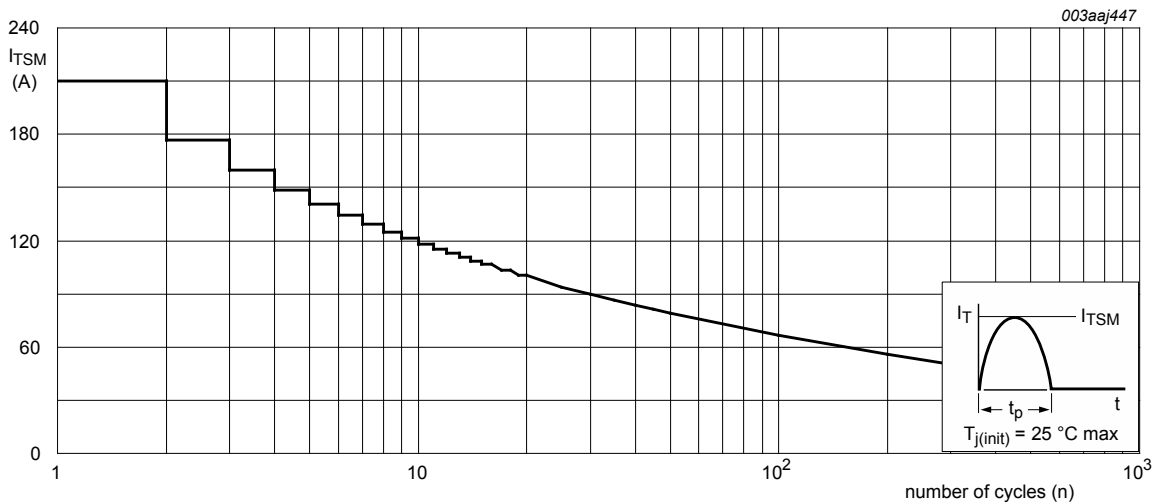
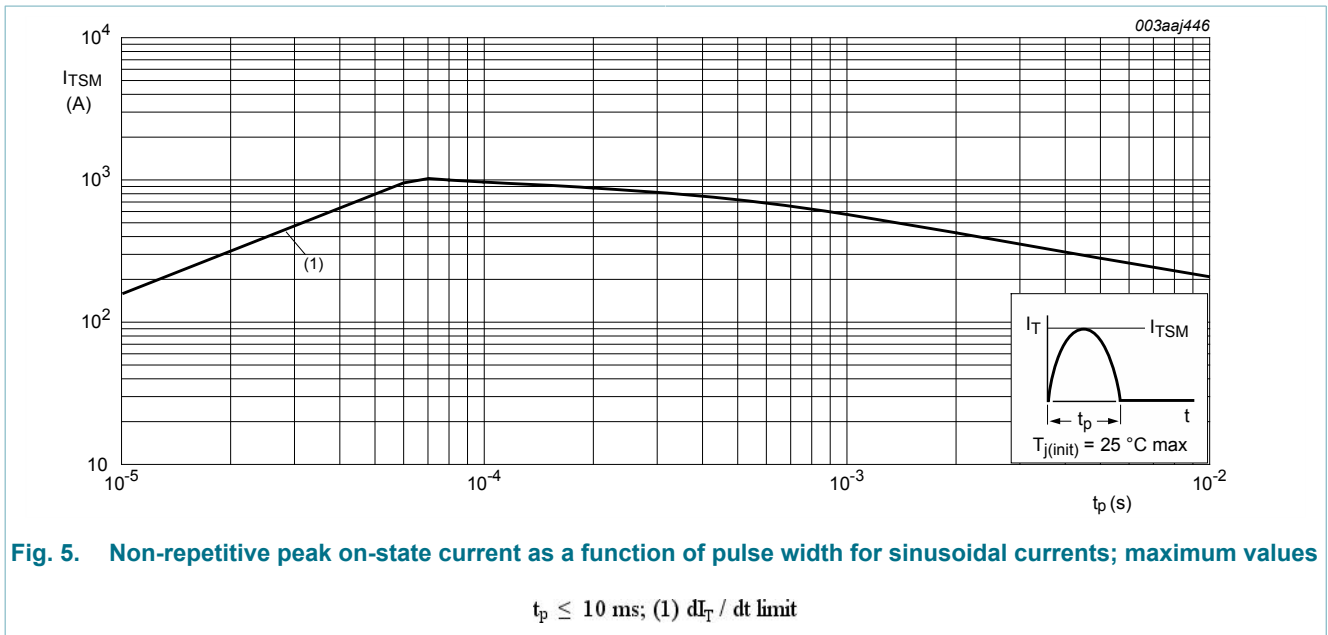


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

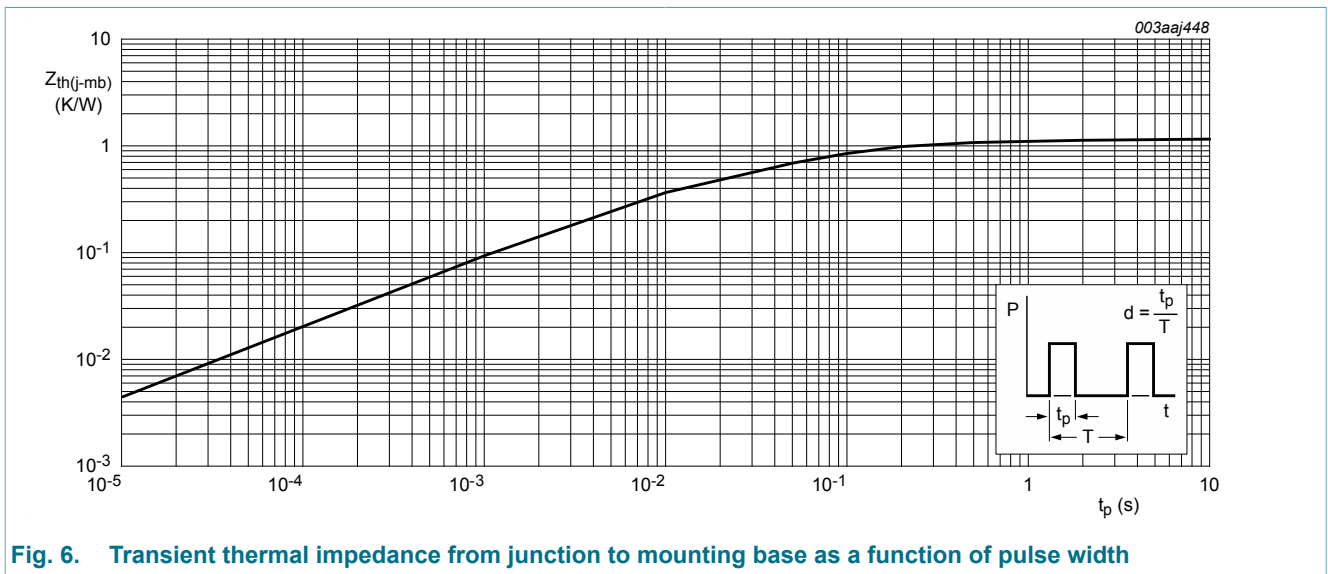
$f = 50 \text{ Hz}$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint, FR4 board	-	55	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	4.5	32	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	21	60	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	16	40	mA
V_T	on-state voltage	$I_T = 32\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.7	1.3	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$; Fig. 11	0.2	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$	-	0.2	1	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$	-	0.2	1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	300	-	-	V/ μs

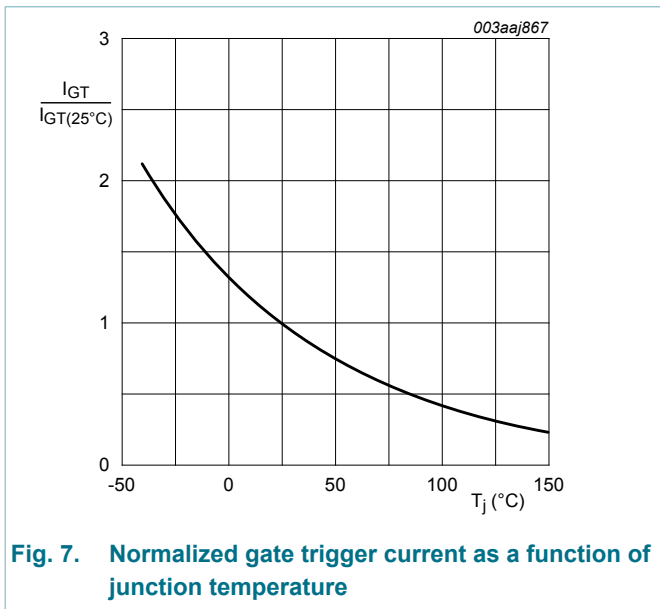


Fig. 7. Normalized gate trigger current as a function of junction temperature

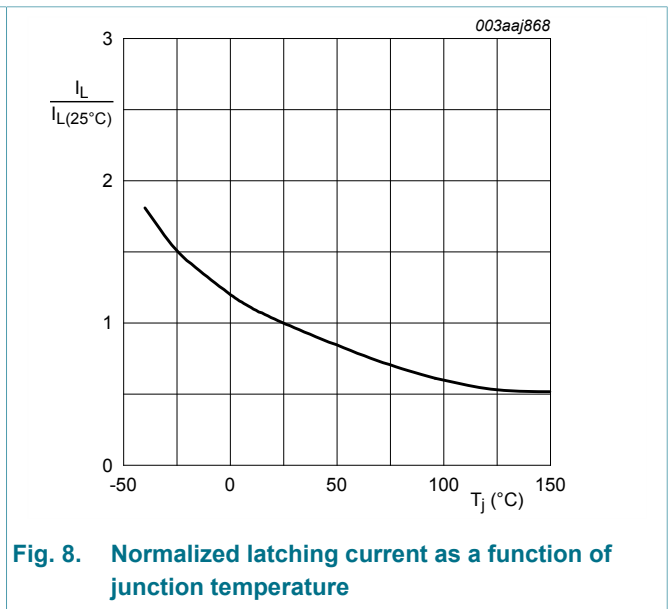


Fig. 8. Normalized latching current as a function of junction temperature

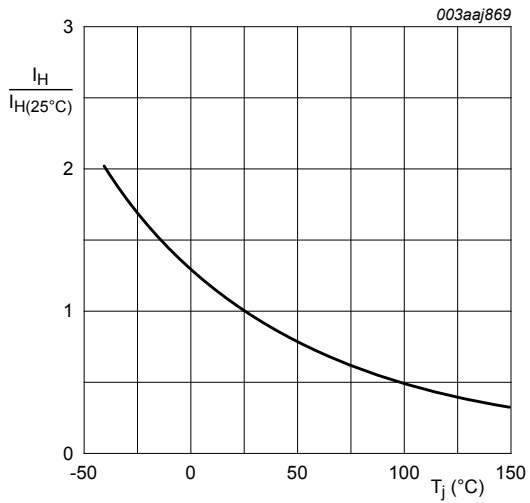
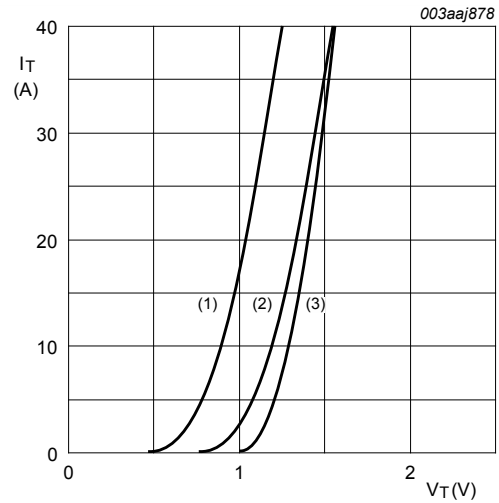


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.0485 \text{ V}$; $R_s = 0.0133 \text{ } \Omega$

- (1) $T_j = 150 \text{ } ^\circ\text{C}$; typical values
- (2) $T_j = 150 \text{ } ^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ } ^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

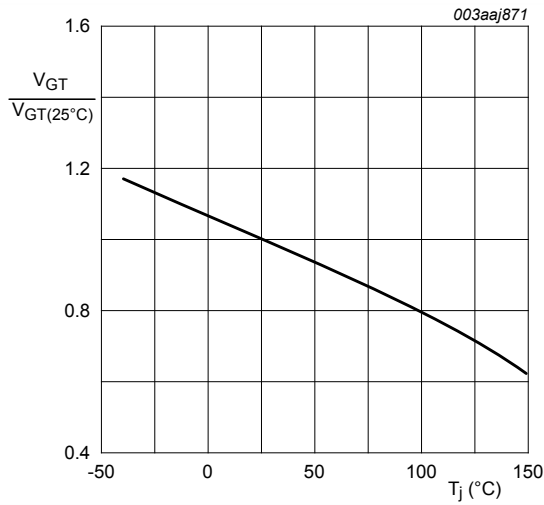
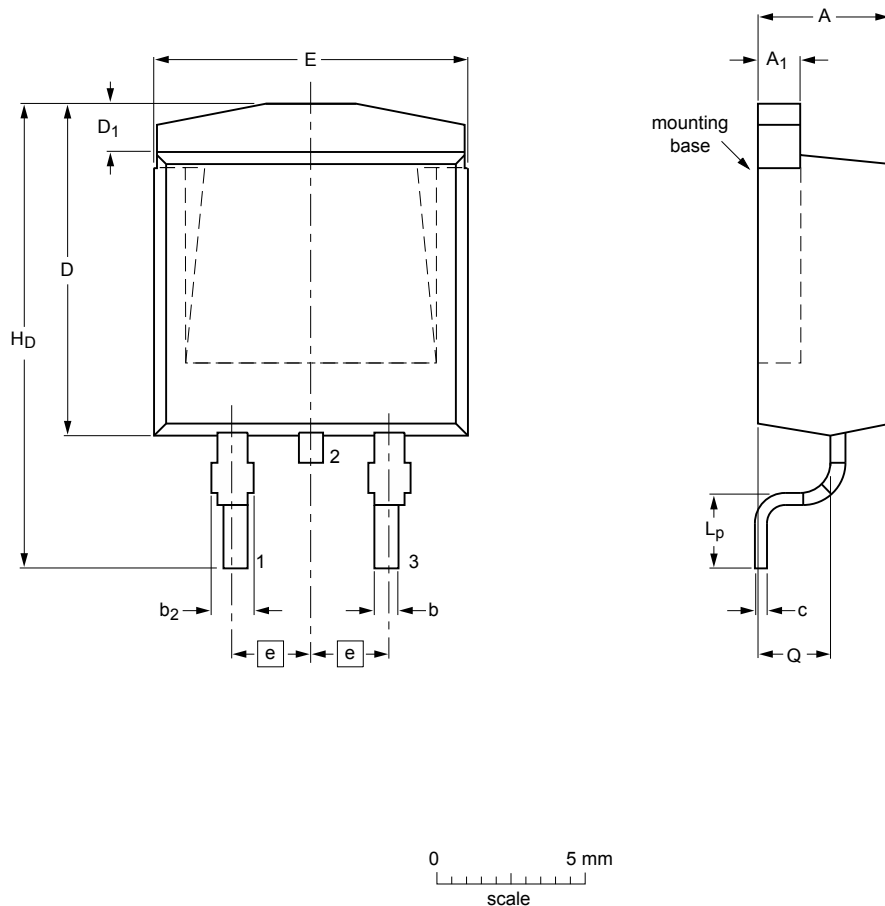


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D	D ₁	E	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 12. Package outline D2PAK (SOT404)

12. Soldering

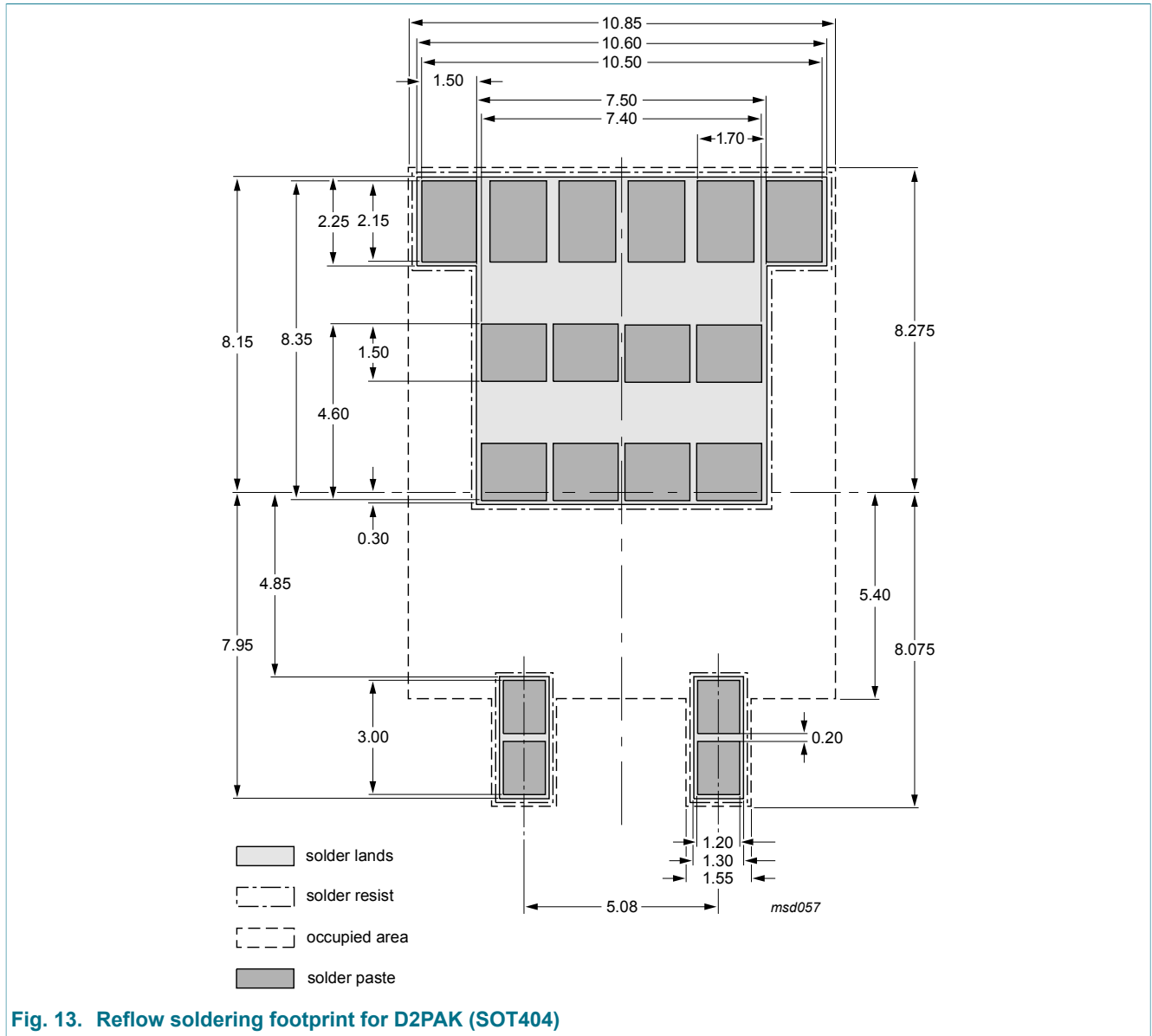


Fig. 13. Reflow soldering footprint for D2PAK (SOT404)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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